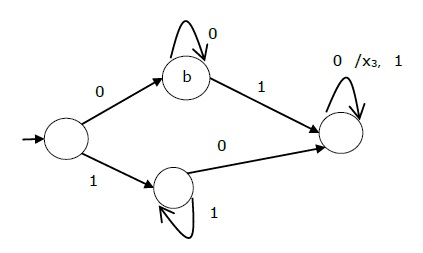
**LAB EXPERIMENT 10**

**Aim:** To design a sequence detector FSM in Xilinx software using Verilog programming. Design a sequence detector that detects a sequence of 1001. It is Mealy type FSM.

**Theory:**

1. Mealy Machine: A Mealy Machine is an FSM whose output depends on the present state as well as the present input.

FSM Diagram:



**Verilog Code of the Program and Outputs:**

1. **Verilog Code of the Program**

module Melaymodel\_062(

    input clk,

    input rst,

    input inp,

    output reg out

    );

reg [1:0] state;

always@(posedge clk or posedge rst)

begin

if(rst)

begin

state<= 2'b00;

out<= 1'b0;

end

else

begin

case(state)

2'b00:begin

      if(inp)

begin

state<=2'b01;

out<= 1'b0;

end

else

begin

state<= 2'b00;

out<= 1'b0;

end

end

2'b00:begin

      if(inp)

begin

state<=2'b01;

out<= 1'b0;

end

else

begin

state<= 2'b00;

out<= 1'b0;

end

end

2'b01:begin

      if(inp)

begin

state<=2'b01;

out<= 1'b0;

end

else

begin

state<= 2'b10;

out<= 1'b0;

end

end

2'b10:begin

      if(inp)

begin

state<=2'b01;

out<= 1'b0;

end

else

begin

state<= 2'b11;

out<= 1'b0;

end

end

2'b11:begin

      if(inp)

begin

state<=2'b01;

out<= 1'b1;

end

else

begin

state<= 2'b00;

out<= 1'b0;

end

end

default begin

state<= 2'b00;

out<= 1'b0;

end

  endcase

     end

end

endmodule

1. **Screenshots of the Program:**

A picture containing text, screenshot, indoor

Description automatically generated

Graphical user interface

Description automatically generated

1. **RTL Schematic:**

A picture containing text, indoor, screenshot, electronics

Description automatically generated

Graphical user interface

Description automatically generated

**Conclusion:** From this experiment we have studies how to make a detector using Mealy Machine. We also learnt how to put delays and check our output on Xilinx ISIM simulator.